

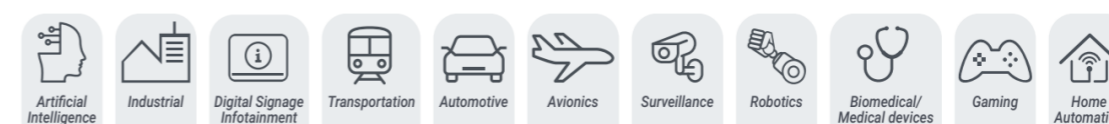
The new i.Core MX8M Plus Fast Ethernet is **based on i.MX 8M Plus** processor equipped with the **quad-core Arm® Cortex®-A53 plus Cortex-M7**. The i.MX 8MP series features offer powerful video processing with an **H.265 video encoder** for efficient compression in live video streaming applications. It runs at **up to 1.8 GHz** with integrated neural processing unit (**NPU**). As the first i.MX processor with **a machine learning accelerator**, it provides high performance for ML inference at the edge.



## HIGHLIGHTS

- Standard Edimm 2.0
- Powerful quad Arm Cortex-A53 processor with a Neural Processing Unit (NPU)
- Suitable for high performance HMI, video and networking applications

## APPLICATIONS



## FEATURES

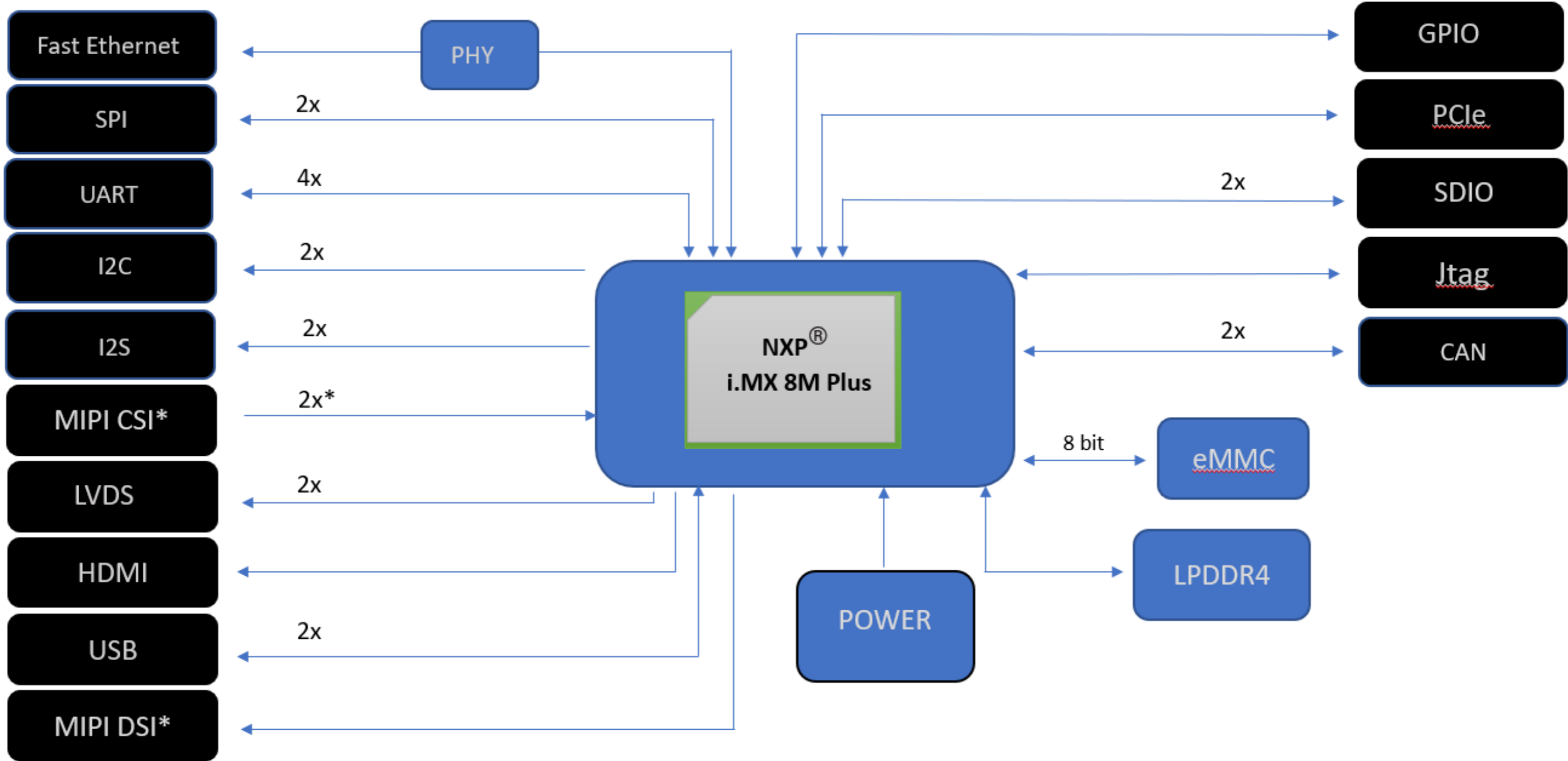


	CPU	NXP® i.MX8M Plus
	CORES	Quad Arm Cortex-A53 @ up to 1.8GHz processor with a (NPU) up to 2.3 TOPS and Cortex-M7 CPU @ 800 MHz.
	MEMORY	Up to 4GB LPDDR4
	GRAPHICS	GC7000UL (2 shaders), OpenGL ES 2.0/3.0/3.1, Vulkan, OpenCL 1.2; GC520 (2D)
	VIDEO INTERFACES	<ul style="list-style-type: none"> <li>• LVDS 18/24bit up to Full HD</li> <li>• HDMI up to Full HD</li> </ul>
	VIDEO PROCESSING	<ul style="list-style-type: none"> <li>• 1080p60 HEVC (h.265, VP9, VP8) dec</li> <li>• 1080p60 HEVC (h.265) enc</li> </ul>
	AUDIO	<ul style="list-style-type: none"> <li>• I<sup>2</sup>S interface</li> </ul>
	NETWORKING	LAN 10/100 Ethernet interfaces

	PCIE	1 x PCIe 3.0
	USB	<ul style="list-style-type: none"> <li>• USB OTG 3.0</li> <li>• USB HOST 3.0</li> </ul>
	MASS STORAGE	Starting from 4GB eMMC drive soldered on-board
	PERIPHERAL INTERFACES	UART, I <sup>2</sup> C, SPI, JTAG, CAN, SDIO, GPIOs
	POWER SUPPLY	+5V DC
	OPERATING SYSTEM	<ul style="list-style-type: none"> <li>• Linux</li> <li>• Yocto</li> <li>• Android</li> </ul>
	OPERATING TEMPERATURE*	Industrial qualified
	DIMENSIONS	32.1 x 67.6 mm

\* Valid for all components except CPU. Customer shall consider junction temperature for CPU. Temperature will widely depend on application. Specific cooling solutions could be necessary for the final system.

BLOCK DIAGRAM



\* The MIPI CSI2 have signals shared with DSI, please see the related chapters on HW Manual for details