GEA STM32MP13 HW MANUAL

GETTING STARTED MANUAL

Revision History

DATE	REVISION	CHANGE DESCRIPTION
07/03/2023	1.0.0	Release

TABLE OF CONTENT

CHAPTER 1

INTRODUCTION

This Chapter gives background information on this document.

Section includes：

- **General Overview**
- **Acronyms and Abbreviations Used**
- **Document and Standard References**

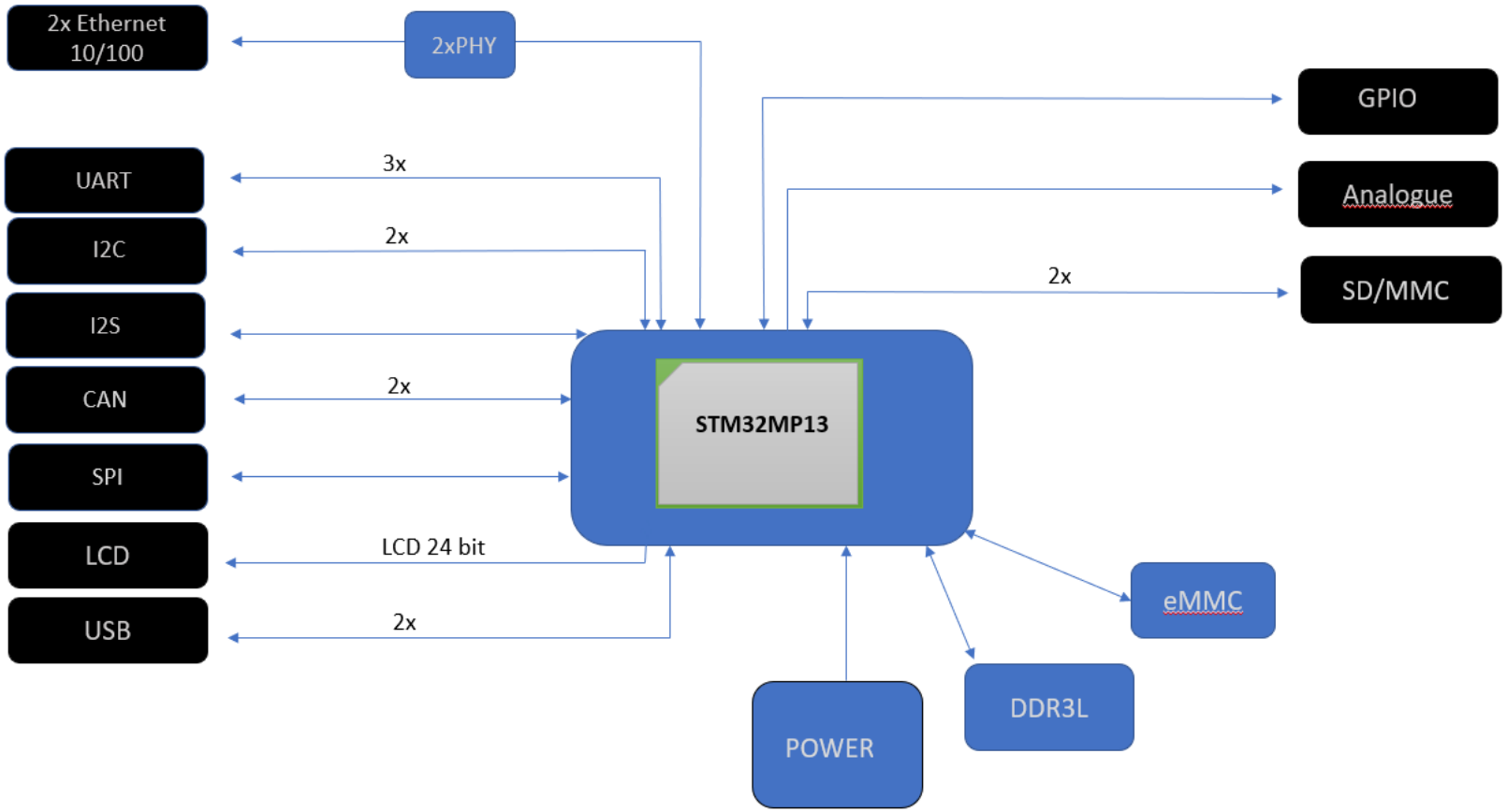
1.1 GENERAL INFORMATION

This document is created to guide users to design ST modules compliant carrier boards. It will focus only on the interfaces in module pinouts and related peripherals.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

All examples of this document are based on carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

1.2 BLOCK DIAGRAM



1.3 MAIN FEATURES

CPU	ST® STM32MP135
CORES	Arm® Cortex®-A7 up to 1 GHz
MEMORY	Up to 1 GB DDR3L - 1066
GRAPHICS	Two layers (incl. 1 secured) with programmable color LUT
VIDEO INTERFACES	LCD-TFT controller, up to 24-bit up to WXGA (1366 × 768) @60 fps
NETWORKING	2x 10/100 Ethernet interfaces
MASS STORAGE	4GB eMMC drive soldered on-board
USB	1 x USB OTG 2.0, 1 x USB HOST 2.0
AUDIO	SAI Interface
PERIPHERAL INTERFACES	UART, I2C, SPI, CAN, SDIO, GPIOs
POWER SUPPLY	+5V DC
OPERATING SYSTEM	• Linux • Yocto
OPERATING TEMPERATURE*	Industrial (-40°C to 85°C)
DIMENSIONS	25 x 67.6 mm

* Valid for all components except CPU. Customer shall consider junction temperature for CPU. Temperature will widely depend on application. Specific cooling solutions could be necessary for the final system.

1.4 DOCUMENT AND STANDARD REFERENCES

1.4.1 EXTERNAL INDUSTRY STANDARD DOCUMENTS

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP).
- USB Specifications (www.usb.org).

1.4.2 OTHER EXTERNAL DOCUMENTS

STM32MP135 Hardware Developer's Guide

STM32MP135lus Reference Manual

STM32MP135lus Data Sheet

1.4.3 ON-LINE DOCUMENTATION

Click on the following link for ST online documentation: ST available documentation

1.5 DISCLAIMER

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1.6 SUPPORT

We offer on-line support to allow the customer to stay updated on the development of software release and on the enhancement of the documentation.

Following is shown the references for ENGICAM on-line support.

www.engicam.com

ENGICAM Product Experts are available to answer questions via email:

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1.7 ACRONYMS AND ABBREVIATIONS USED

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDMI	High-Definition Multimedia Interface, combines audio and video signal
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

CHAPTER 2

MECHANICAL DATA

This Chapter gives information about PCB and module's dimensions.

Section includes：

- **Assembly Top View**
- **Assembly Bottom View**
- **Mechanical data**

2.1 MECHANICAL DATA

The ST module has a standard SO DIMM footprint compliant with TYCO ELECTRONICS code 1473005-1 or compatible connector. The PCB dimensions is L 67.60 x W 25 x H 1 mm. The distances available on PCB under the module are from **1** to 1.4 mm

2.1.1 ASSEMBLY TOP VIEW

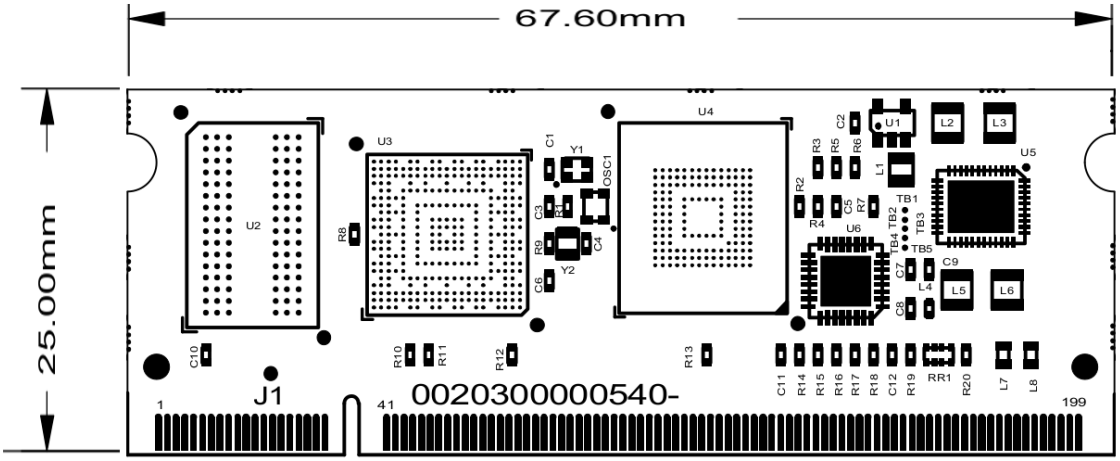


Figure 1

2.1.2 ASSEMBLY BOTTOM VIEW

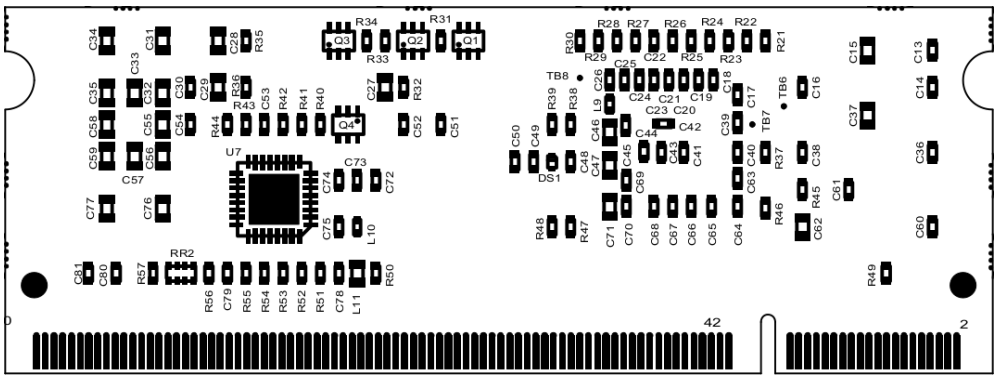


Figure 2

CHAPTER 3

ORDERING INFORMATION

This Chapter gives the ordering information and technical specifications of the modules.

Section includes：

- **GEA STMP1 ordering codes**
- **CPU & Memory specification**
- **Operating temperature range**
- **STM32MP135 supported features**

3.1 ORDERING INFORMATION

Following is provided the ordering information and the description for the Basic technical specifications modules:

Marking Code	Ordering Code	MPQ	Description	CPU & Memory specifications	Operating temperature range °C (excepted CPU)	Module available at least until [1]
GEA STM32MP1 512 FULL	002682028DI43A	1	EDIMM 2.0 STM32MP135 1GHz, 512MB DDR3, Industrial, 4GB **eMMC -25°C**, dual Ethernet 10/100	STM32MP135DAF7 Industrial Temperature Cortex-A7 @ up to 1 GHz, -40 to +105C [2], 4GB eMMC **-25°C**, 16 bit DDR3L, temperature range Industrial	-25 to +85	4thQ -2033
GEA STM32MP1 512 FULL	002672028DI43A	58			-25 to +85	4thQ -2033
GEA STM32MP1 512 FULL Secure	002682028DI43A	1	EDIMM 2.0 STM32MP135 1GHz, 512MB DDR3, Industrial, 4GB **eMMC -25°C**, dual Ethernet 10/100	STM32MP135FAF7 Industrial Temperature Cortex-A7 @ up to 1 GHz, -40 to +105C [2], 4GB eMMC **-25°C**, 16 bit DDR3L, temperature range Industrial	-25 to +85	4thQ -2033
GEA STM32MP1 512 FULL Secure	002672028DI43A	58			-25 to +85	4thQ -2033

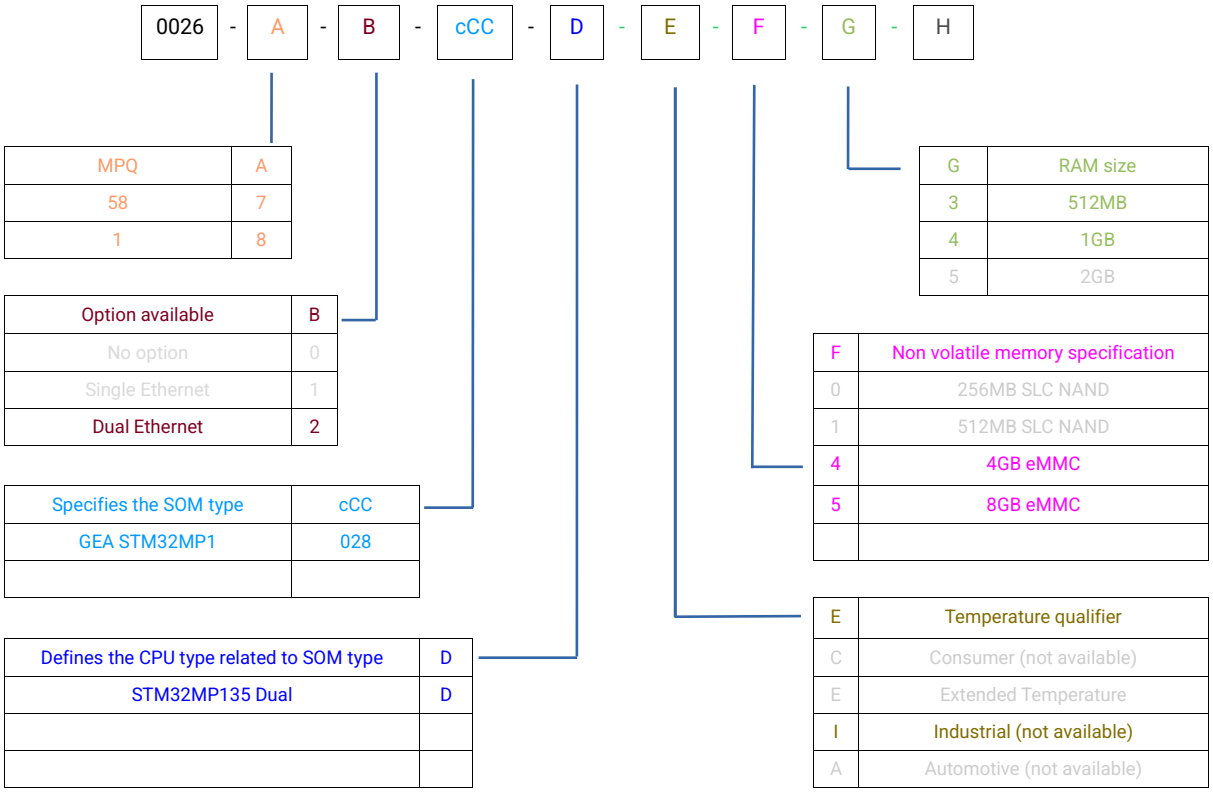
Table 1

[1] *Long Term Availability based on ST longevity program*
[2] *Note: internal junction temperature (for further information see ST documentation)*

WARNING: the actual temperature depends on the application, the enclosure and/or the environmental condition. Upon customer to consider specific cooling solutions for its own final system.

3.2 PART NUMBER STRUCTURE

The module is available with eMMC option. *The standard order codes shown in the tables above shall be modified as follow:*



WARNING: not all the custom configurations might be available in respect of standard times and orderable quantities

CHAPTER 4

PINOUT AND ELECTRICAL SPECS

This Chapter gives the pinout information.

Section includes：

- **Pinout overview**
- **Pad specifications**
- **Electrical specifications**

4.1 MODULE PINOUT

The module's interface is achieved by a SO DIMM 200 position connector TYCO ELECTRONICS code 1473005-1 or compatible

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
1	+1V8	-	Output Power PIN	-	-
2	+1V8	-	Output Power PIN	-	-
3	GND	-	Power PIN	N	-
4	GND	-	Power PIN	N	-
5	GND	-	Power PIN	N	-
6	PE8	PE8	Spare GPIO	Y	+3,3V
7	PA14	PA14	Spare GPIO	Y	+3,3V
8	PF10	PF10	Spare GPIO	Y	+3,3V
9	PB7	PB7	Spare GPIO	Y	+3,3V
10	PB8	PB8	Spare GPIO	Y	+3,3V
11	PA13	PA13	Spare GPIO	Y	+3,3V
12	PE5	PE5	Spare GPIO	Y	+3,3V
13	PE6	PE6	Spare GPIO	Y	+3,3V
14	PE11	PE11	Spare GPIO	Y	+3,3V
15	PF13	PF13	Spare GPIO	Y	+3,3V
16	PF14	PF14	Spare GPIO	Y	+3,3V
17	PF15	PF15	Spare GPIO	Y	+3,3V
18	+Vcoin [3)]	-	Backup battery or RTC	-	-
19	NC	-	-	-	-
20	NC	-	-	-	-
21	NC	-	-	-	-
22	GND	-	Power PIN	N	-
23	I2C1_SCL	PD1	I2C SCL Signal	Y	+3,3V
24	I2C1_SDA	PH6	I2C SDA Signal	Y	+3,3V
25	ADC2_INP3	PA1	ADC Signal	Y	+3,3V
26	ADC2_INN3	PA0	ADC Signal	Y	+3,3V
27	SPI1_NSS	PF12	SPI Chip Select signal	Y	+3,3V
28	SPI1_MOSI	PA3	SPI MOSI signal	Y	+3,3V
29	SPI1_MISO	PA6	SPI MISO signal	Y	+3,3V
30	SPI1_SCK	PB1	SPI CLK signal	Y	+3,3V
31	GND	-	Power PIN	N	-
32	PD13	PD13	Spare GPIO	Y	+3,3V
33	PH3	PH3	Spare GPIO	Y	+3,3V
34	SAI1_MCLKA	PC3	I2S Master Clock	Y	+3,3V
35	PH5	PH5	Spare GPIO	Y	+3,3V
36	PH7	PH7	Spare GPIO	Y	+3,3V
37	PI0	PI0	Spare GPIO	Y	+3,3V
38	PI1	PI1	Spare GPIO	Y	+3,3V

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
39	GND	-	Power PIN	-	-
40	PI2	PI2	Spare GPIO	Y	+3,3V
41	NC	-	-	-	-
42	NC	-	-	-	-
43	NC	-	-	-	-
44	NC	-	-	-	-
45	NC	-	-	-	-
46	NC	-	-	-	-
47	NC	-	-	-	-
48	NC	-	-	-	-
49	NC	-	-	-	-
50	NC	-	-	-	-
51	NC	-	-	-	-
52	NC	-	-	-	-
53	NC	-	-	-	-
54	NC	-	-	-	-
55	NC	-	-	-	-
56	NC	-	-	-	-
57	NC	-	-	-	-
58	NC	-	-	-	-
59	NC	-	-	-	-
60	NC	-	-	-	-
61	NC	-	-	-	-
62	NC	-	-	-	-
63	SPI2_MOSI	PH10	SPI MOSI signal	Y	+3,3V
64	GND	-	Power PIN	N	-
65	PC0	PC0	Spare GPIO	Y	+3,3V
66	PB0	PB0	Spare GPIO	Y	+3,3V
67	NC	-	-	-	-
68	SPI2_NSS	PB13	SPI Chip Select signal	Y	+3,3V
69	NC	-	-	-	-
70	NC		-	-	-
71	GND	-	Power PIN	N	-
72	SPI2_CLK	PB10	SPI CLK signal	Y	+3,3V
73	SPI2_MISO	PB5	SPI MISO signal	Y	+3,3V
74	NC	-	-	-	-
75	NC	-	-	-	-
76	NC	-	-	-	-
77	NC	-	-	-	-
78	NC	-	-	-	-
79	NC	-	-	-	-
80	nSD_BOOT[2)]	-	-	-	+3,3V

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
81	NC	-	-	-	-
82	LCD_B0	PH2	LCD interface	Y	+3,3V
83	NC	-	-	-	-
84	LCD_B1	PE13	LCD interface	Y	+3,3V
85	NC	-	-	-	-
86	LCD_G0	PF5	LCD interface	Y	+3,3V
87	NC	-	-	-	-
88	LCD_G1	PF1	LCD interface	Y	+3,3V
89	GND	-	Power PIN	N	-
90	LCD_R0	PA15	LCD interface	Y	+3,3V
91	NC	-	-	-	-
92	LCD_R1	PG7	LCD interface	Y	+3,3V
93	NC	-	-	-	-
94	ETH2_TXP	-	Fast Ethernet TXP signal	-	-
95	NC	-	-	-	-
96	ETH2_TXN	-	Fast Ethernet TXN signal	-	-
97	ETH2_LED_10_100_ KATHOD	-	Led Indicator Cathode signal	-	-
98	ETH2_RXP	-	Fast Ethernet RXP signal	-	-
99	ETH2_LED_ACT_ KATHOD	-	Led indicator Cathode signal	-	-
100	ETH2_RXN	-	Fast Ethernet RXN signal	-	-
101	NC	-	-	-	-
102	NC	-	-	-	-
103	NC	-	-	-	-
104	NC	-	-	-	-
105	USART2_RTS	PD4	UART2 CTS signal	Y	+3,3V
106	USART2_CTS	PE15	UART2 RTS signal	Y	+3,3V
107	GND	-	Power PIN	N	-
108	USART2_TX	PH12	UART2 TXD signal	Y	+3,3V
109	USART2_RX	PD15	UART2 RXD signal	Y	+3,3V
110	I2C2_SDA	PG9	I2C SDA Signal	Y	+3,3V
111	I2C2_SCL	PD7	I2C SCL Signal	Y	+3,3V
112	UART8_TX	PE1	UART2 TXD signal	Y	+3,3V
113	UART8_RX	PF9	UART2 RXD signal	Y	+3,3V
114	SAI1_SDB	PG10	I2S Data In	Y	+3,3V
115	SAI1_FSA	PF11	I2S RCLK	Y	+3,3V
116	UART4_TX	PD6	UART1 TXD signal	Y	+3,3V
117	UART4_RX	PD8	UART1 RXD signal	Y	+3,3V
118	CAN1_TX	PE10	CAN 1 transmit signal	Y	+3,3V
119	CAN1_RX	PD0	CAN 1 receive signal	Y	+3,3V
120	CAN2_TX	PG1	CAN 2 transmit signal	Y	+3,3V
121	CAN2_RX	PG3	CAN 2 receive signal	Y	+3,3V
122	SAI1_SDA	PA5	I2S Data Out	Y	+3,3V

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
123	GND	-	Power PIN	N	-
124	SAI1_SCKA	PA4	I2S SCLK	Y	+3,3V
125	LCD_CLK	PD9	LCD interface	Y	+3,3V
126	NC	-	-	-	-
127	ETH1_TXN	-	Fast Ethernet TXN signal	-	-
128	nRESET		Reset signal	N	+3,3V
129	ETH1_TXP	-	Fast Ethernet TXP signal	-	-
130	PI3	PI3	Spare GPIO	Y	+3,3V
131	ETH1_RXN	-	Fast Ethernet RXN signal	-	-
132	LCD_BL	PE12	LCD interface	Y	+3,3V
133	ETH1_RXP	-	Fast Ethernet RXP signal	-	-
134	+3V3_AUX	-	Output Power PIN	N	-
135	+3V3_AUX	-	Output Power PIN	N	-
136	NC	-	-	-	-
137	ETH1_LED_ ACT_ KATHOD	-	Led Indicator Anode signal	-	-
138	NC	-	-	-	-
139	ETH1_LED_10_100_KATHOD	-	Led indicator Cathode signal	-	-
140	+3V3_AUX	-	Output Power PIN	-	-
141	LCD_R7	PD11	LCD interface	Y	+3,3V
142	LCD_R6	PA9	LCD interface	Y	+3,3V
143	LCD_R5	PE7	LCD interface	Y	+3,3V
144	LCD_R4	PD14	LCD interface	Y	+3,3V
145	LCD_R3	PB12	LCD interface	Y	+3,3V
146	LCD_R2	PH8	LCD interface	Y	+3,3V
147	LCD_G7	PE4	LCD interface	Y	+3,3V
148	LCD_G6	PH10	LCD interface	Y	+3,3V
149	LCD_G5	PG0	LCD interface	Y	+3,3V
150	LCD_G4	PD5	LCD interface	Y	+3,3V
151	LCD_G3	PF3	LCD interface	Y	+3,3V
152	LCD_G2	PH13	LCD interface	Y	+3,3V
153	LCD_B7	PA8	LCD interface	Y	+3,3V
154	LCD_B6	PB6	LCD interface	Y	+3,3V
155	LCD_B5	PE0	LCD interface	Y	+3,3V
156	GND	-	Power PIN	N	-
157	LCD_B4	PH14	LCD interface	Y	+3,3V
158	LCD_B3	PF2	LCD interface	Y	+3,3V
159	LCD_B2	PD10	LCD interface	Y	+3,3V
160	LCD_VSYNC	PG4	LCD interface	Y	+3,3V
161	LCD_HSYNC	PE9	LCD interface	Y	+3,3V
162	LCD_DRDY	PH9	LCD interface	Y	+3,3V
163	NC	-	-	-	-
164	NC	-	-	-	-

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
165	NC	-	-	-	-
166	SDIO_B_DATA3 [1)]	PC11	SD DAT 3 signal	Y	+3,3V
167	SDIO_B_CMD [1)]	PD2	SD CMD signal	Y	+3,3V
168	SDIO_B_DATA0 [1)]	PC8	SD DAT 0 signal	Y	+3,3V
169	SDIO_B_CLK [1)]	PC12	SD CLK signal	Y	+3,3V
170	SDIO_B_DATA2 [1)]	PC10	SD DAT 2 signal	Y	+3,3V
171	SDIO_B_DATA1 [1)]	PC9	SD DAT 1 signal	Y	+3,3V
172	NC	-	-	-	-
173	NC	-	-		-
174	NC	-	-		-
175	NC	-	-		-
176	NC	-	-		-
177	NC	-	-		-
178	NC	-	-		-
179	NC	-	-		-
180	NC	-	-		-
181	BOOT_MODE	BOOT_MODE	Boot from USB UART or on board Nand Flash	-	-
182	GND	-	Power PIN	N	-
183	SDIO_A_nCD	PH4	SD CD Signal	Y	+3,3V
184	PA7	PA7	Spare GPIO - uSDHC1 WP Signal	Y	+3,3V
185	SDIO_A_D3 [1)]	PC11	uSDHC1 DAT 3 signal	Y	+3,3V
186	SDIO_A_D2 [1)]	PC10	uSDHC1 DAT 2 signal	Y	+3,3V
187	SDIO_A_D1 [1)]	PC9	uSDHC1 DAT 1 signal	Y	+3,3V
188	SDIO_A_D0 [1)]	PC8	uSDHC1 DAT 0 signal	Y	+3,3V
189	SDIO_A_CK [1)]	PC12	uSDHC1 CLK signal	Y	+3,3V
190	SDIO_A_CMD [1)]	PD2	uSDHC1 CMD signal	Y	+3,3V
191	USB_OTG_ID	PA10	USB on the go interface	Y	+3,3V
192	USB_OTG_DP	USB_DP2	USB on the go interface	N	-
193	USB_OTG_DN	USB_DM2	USB on the go interface	N	-
194	USB_H1_DP	USB_DP1	USB HOST interface	N	-
195	USB_OTG_VBUS	OTG_VBUS	USB on the go interface	N	-
196	USB_H1_DN	USB_DM1	USB HOST interface	N	-
197	+5Vin	-	Power PIN	N	-
198	+5Vin	-	Power PIN	N	-
199	+5Vin	-	Power PIN	N	-
200	+5Vin	-	Power PIN	N	-

Table 2

The yellow rows highlight the required minimum electrical connections in order to make the module working correctly.

[1)] **These pins are mapped on the same PADS, so the SDIO A and B are CANNOT be used simultaneously**
[2)] *Note: for the use of this pin refer to boot option in "**Boot Mode Pin**" chapter*
[3)] *Connect to Coin-Cell or Super-Cap; left floating if not used*

4.2 ELECTRICAL SPECIFICATIONS

4.2.1 OPERATING RANGES

All the values reported in the following table have to be confirmed

	V Min (Volts)	V Typ (Volts)	V Max (Volts)
Vin 1)	-	+ 5	+ 5,25
VBUS_USB (180, 195)	-	+ 5	+ 5,25
GPIO V(oh)	+ 2,8	-	-
GPIO V(ol)	-	-	+ 0,4
GPIO V(ih)	+ 2,3		+ 3,3
GPIO V(il)	0	-	+ 0,6
GPIO V($oh_{1.8v}$)	+ 1,6	-	+ 1,8
GPIO V($ol_{1.8v}$)	-	-	+ 0,36
GPIO V($ih_{1.8v}$)	+ 1,25		+ 1,8
GPIO V($il_{1.8v}$)	0	-	+ 0,35

Table 3

1) *This measure has done testing the module's start at the limit temperatures of -40°C and +85°C*

4.2.2 POWER CONSUMPTION

The current consumption has to be still measured

Module	Test condition	Current @ V Min	Current @ V Typ	Current @ V Max
GEA STMP1	Linux Sleep mode	-	-	-
	Linux Wayland Running	-	-	-
		-	-	-

Table 4

CHAPTER 5

MODULE INTERFACES

This Chapter gives the technical specifications for carrier board design.

Section includes：

- **Power signals and backup battery**
- **Serials**
- **CAN Bus**
- **Ethernet**
- **USB**
- **SDIO**
- **LCD**
- **LVDS**
- **Boot mode**
- **Audio**
- **Reset pin management**

5.1 HOW TO POWER THE MODULE

Read carefully the related sections before starting the power stage design. This module needs to be supply up to +5Vin power. Please refer to the table below for the power supply range specification. The power dissipated by the module in the operating mode is up to 600 mA, but **the system must provide at least a power of 2A at 5V to allow the start of the module.**

The following table shows the module power supply pins numbering, please connect all power supply pins in order to avoid damage.

Number	Name	Primary Function Description	GPIO Capable	Voltage
197	+5Vin	Power PIN	N	-
198	+5Vin	Power PIN	N	-
199	+5Vin	Power PIN	N	-
200	+5Vin	Power PIN	N	-
3	GND	Power PIN	N	-
4	GND	Power PIN	N	-
5	GND	Power PIN	N	-
22	GND	Power PIN	N	-
31	GND	Power PIN	N	-
39	GND	Power PIN	N	-
64	GND	Power PIN	N	-
71	GND	Power PIN	N	-
89	GND	Power PIN	N	-
107	GND	Power PIN	N	-
123	GND	Power PIN	N	-
156	GND	Power PIN	N	-
182	GND	Power PIN	N	-

Table 5

ST module has 5 Output power PIN usable for power source. The table below shows the power supply pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
1	+1V8	Output Power PIN	N	-
2	+1V8	Output Power PIN	N	-
134	+3V3_OUT	Output Power PIN	N	-
135	+3V3_OUT	Output Power PIN	N	-
140	+3V3_OUT	Output Power PIN	N	-

Table 6

The following table shows the nominal maximum rating of power output:

Power output	Max output current
+1V8	50 mA (Total)
+3V3_OUT	800 mA (Total)

Table 7

WARNING!

The currents above 600 mA provided by the +3V3_OUT of the module, help to lower the performance in temperature.
We recommend adding a regulator voltage for an external current greater than or equal to 600 mA, in those applications where the operating temperature range is important.

For further details on the power supply refer to ST data sheet and Reference Manual.

5.2 HOW TO CONNECT A BACKUP BATTERY

The module allows the use of lithium rechargeable battery or supercapacitor as backup battery.
The connection with module is obtained by connecting directly the backup battery to the +Vcoin signal (pin 18 floating if not used).

Warning: the consumption of the RTC of the SOM is still under processing, an external RTC (on carrier board) may be the recommended solution.

Note: *The module is already designed to manage the charge of backup battery.*

5.3 HOW TO CONNECT TWO 3-WIRE RS232 SERIAL PORT

This section shows how to use the ST UARTs as 3-wire RS232 serial ports. The table shows involved UARTs and the associated pins:

Number	Name	Primary Function Description	GPIO Capable	Voltage
112	UART8_TXD	UART8 TXD signal	Y	+3,3V
113	UART8_RXD	UART8 RXD signal	Y	+3,3V
116	UART4_TXD	UART4 TXD signal	Y	+3,3V
117	UART4_RXD	UART4 RXD signal	Y	+3,3V

Table 8

The signals on the module's UART pins are 3.3V logic level, this cannot be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

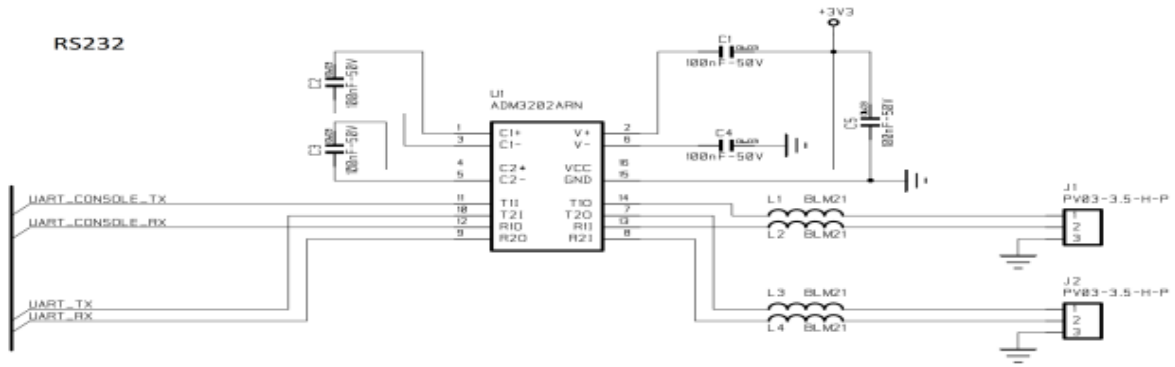


Figure 3

The figure shows how to connected the UART of the ST using an RS232 transceiver. In the example an ADM3202ARN IC from Analog Device, is used like transceiver for both UARTs channels without any control signal. In case RTS and CTS are need, a transceiver must be used for these signals.

When Linux is installed on a module, UART4 is used like console. The default communications settings are shown in the table below.

Linux console default settings	
Baud rate	115200
Data length	8 bit
Parity	none
Stop	1bit

Table 9

* **Note**: in the GEA STMP1 module *the UART4 is used as Linux Console*

5.4 HOW TO CONNECT A RS485 SERIAL PORT

This chapter shows how an RS485 serial port can be connected to the module. The figure below shows how UART is connect to the RS485 transceiver.

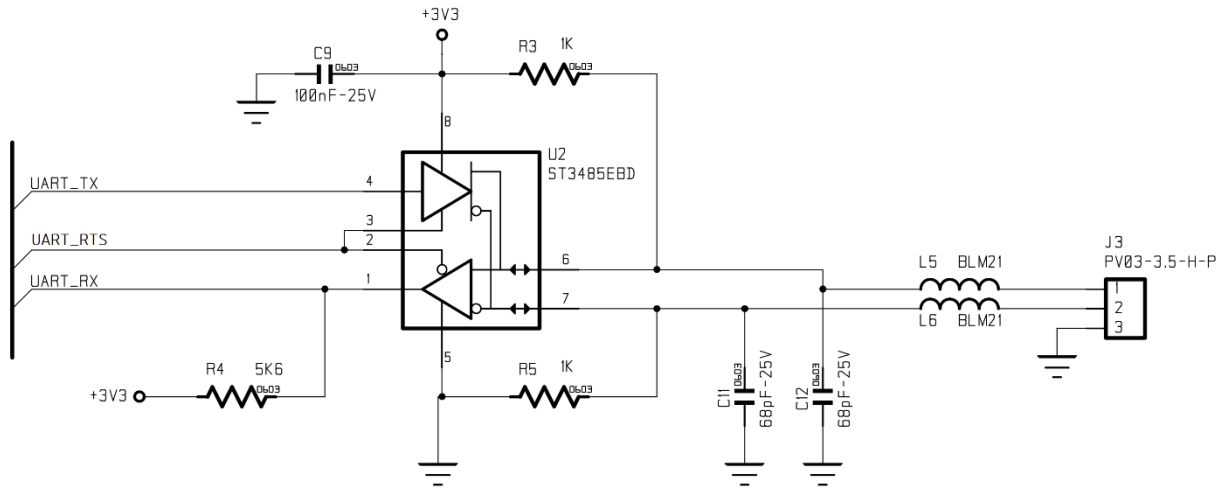


Figure 4

The pins involved in this RS485 communication in standard EDIMM spec are listed in the following table.

Number	Name	Primary Function Description	GPIO Capable	Voltage
105	USART2_RTS_OUT	UART2 RTS signal (Output)	Y	+3,3V
106	USART2_CTS_IN	UART2 CTS signal (Input)	Y	+3,3V
108	USART2_TX	UART2 TXD signal (Output)	Y	+3,3V
109	USART2_RX	UART2 RXD signal (Input)	Y	+3,3V

Table 10

5.5 HOW TO CONNECT CAN BUS INTERFACES

This chapter describes how CAN bus transceiver can be connected to the STM32MP135 module.

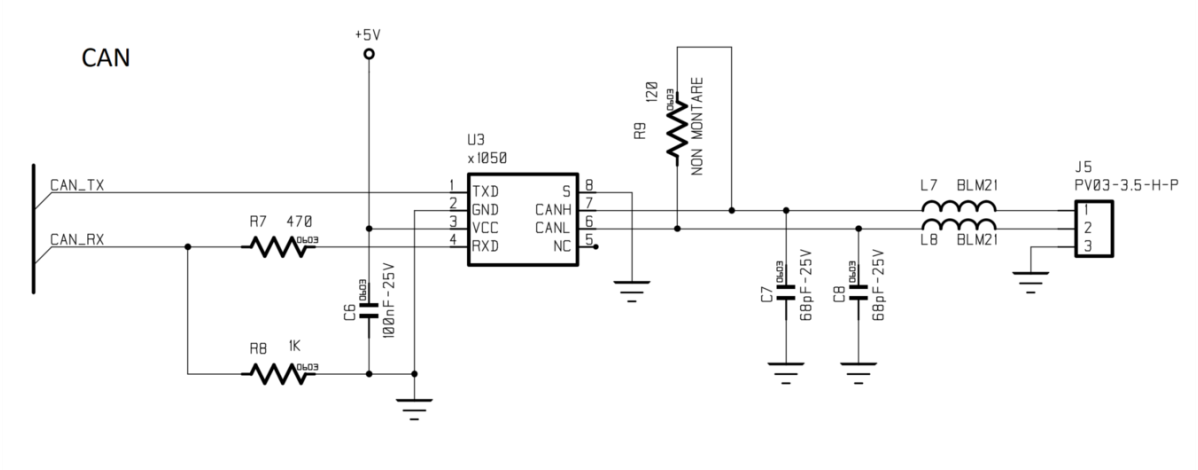


Figure 5

The following table describes the pins' numbering in the main connector involved in the CAN interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
118	CAN1_TX	CAN 1 transmit signal	Y	+3,3V
119	CAN1_RX	CAN 1 receive signal	Y	+3,3V
120	CAN2_TX	CAN 2 transmit signal	Y	+3,3V
121	CAN2_RX	CAN 2 receive signal	Y	+3,3V

Table 11

Usually, a Jumper is used to close the load of the CAN Bus to 120 Ω

5.6 HOW TO DESIGN THE ETHERNET INTERFACE

5.6.1 DOUBLE ETHERNET OPTION (2 X PHY ON BOARD)

The NXP ST Ethernet Media Access Controller (MAC) is designed to support 2 x 10/100 Mbps Ethernet/IEEE standard 802.3™ networks.

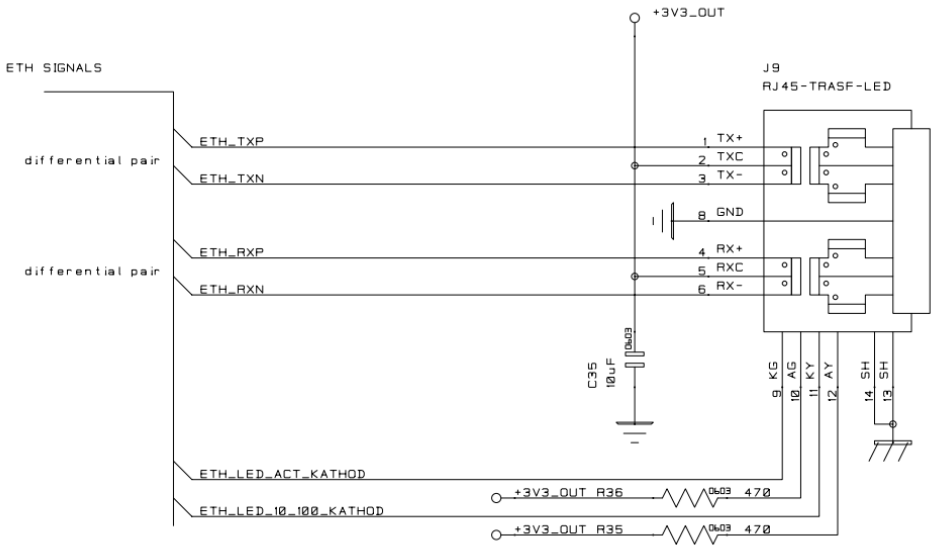


Figure 6

The table below lists both the Ethernet signals available on the module.
The primary function description is referred to the differential pair in 1000BASE-T mode.

Number	Name	Primary Function Description	GPIO Capable	Voltage
127	ETH1_TXN	Fast Ethernet TXN signal	-	+3,3V
129	ETH_TXP	Fast Ethernet TXP signal	-	+3,3V
131	ETH1_RXN	Fast Ethernet RXN signal	-	+3,3V
133	ETH1_RXP	Fast Ethernet RXP signal	-	+3,3V
137	ETH1_LED_ ACT_ KATHOD	Led Indicator Cathode signal	-	+3,3V
139	ETH1_LED_10_100_KATHOD	Led indicator Cathode signal	-	+3,3V

Table 12

Number	Name	Primary Function Description	GPIO Capable	Voltage
96	ETH2_TXN	Fast Ethernet TXN signal	-	+3,3V
94	ETH2_TXP	Fast Ethernet TXP signal	-	+3,3V
100	ETH2_RXN	Fast Ethernet RXN signal	-	+3,3V
98	ETH2_RXP	Fast Ethernet RXP signal	-	+3,3V
99	ETH2_LED_ ACT_ KATHOD	Led Indicator Cathode signal	-	+3,3V
97	ETH2_LED_10_100_KATHOD	Led indicator Cathode signal	-	+3,3V

Table 13

[1] ***Note:*** In 10BASE-T/100BASE-TX these pins are not to be used

5.6.2 COMPONENT PLACEMENT CONSIDERATIONS

Components placement can affect signal quality, emissions and can decrease EMI problems.

1. If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
2. To decrease EMI problems the distance between magnetics and Phy should be at least 25mm or greater to isolate the PHY from magnetics.
3. The distance between Phy and RJ45 connector should always be within 200 mm.
4. The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector, away from the board of PCB.
5. The signals RX & TX should be independently matched in length to within 3 mm

See following figure

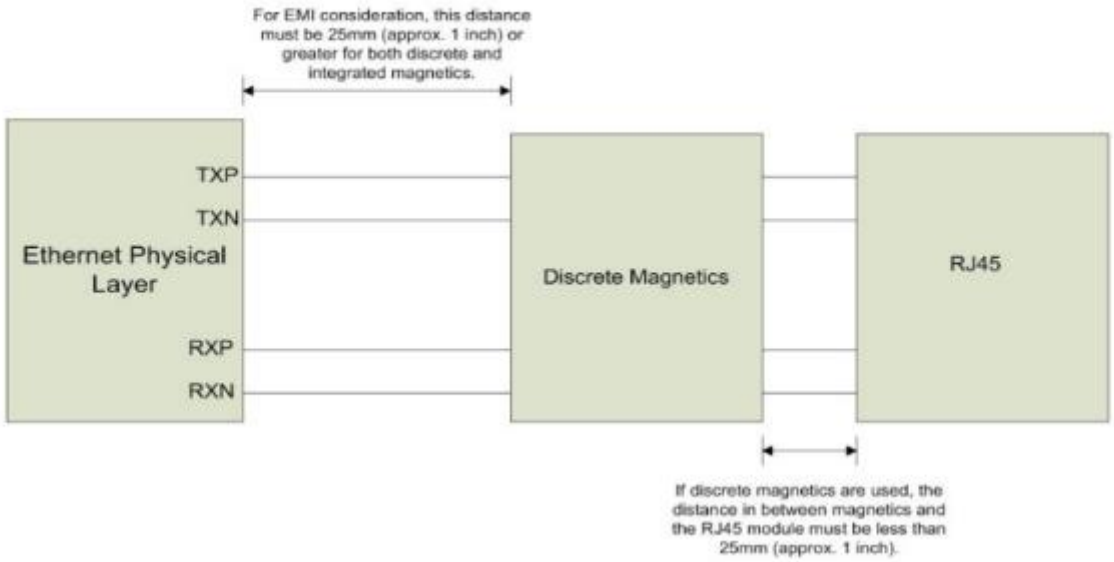


Figure 7

The PHY used in the module is the SMSC LAN8710.
For more information refer to the SMSC Ethernet Physical Layer Layout Guidelines.
For a list of magnetics selected to operate with the SMSC LAN8710, refer to the Application note AN 8-13 Suggested Magnetics.
WARNING:
The second LAN8710 is assembled only in the module FULL version

** Figure 2.3 from SMSC Ethernet Physical Layer Layout Guidelines*

5.6.3 CABLE TRANSIENT EVENT AND PHY PROTECTION

Cable transient events are + and - DC surges that are induced across the transformer onto the PHY side of the TX+/- and RX+/- signals as shown in the figure below. The PHY side of the transformer should not contain any DC component other than the typical 3.3V pull-up on the center tap of the transformer for analog signal biasing. Especially in POE applications, there are two main reasons why cable transient events occur, negative rail PSE switching, and hot unplug/plug-in events.

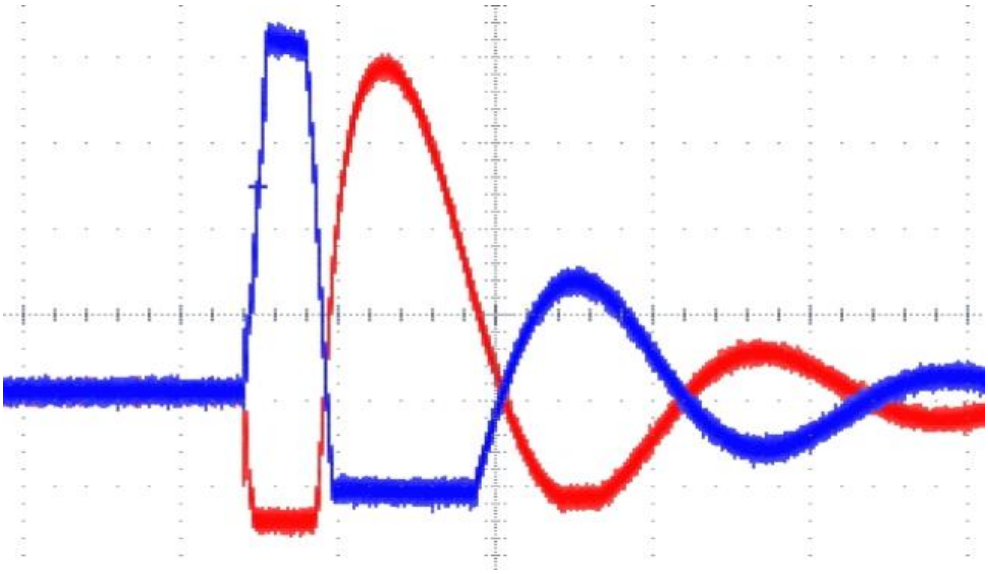


Figure 8

Transient observer on the PHY side of Eth Magnetics

Scale X = 1uS/div

Scale Y = 5V/div

Note: *for further details about Cable transient events refer to file AN1718 of SMSC*

5.6.4 PHY ETHERNET

When using an SMSC device, for each application an external transient protection is recommended , especially when the POE is used, as shown in the figure below. The schematic shows an example of a TVS suppression solution. This solution couples the energy differentially into the two TVS diodes on each differential pair. For cases when the transient is across the TX+/- pair in the figure below, the voltage is clamped at a value equivalent to the forward bias voltage across D1, plus the zener voltage of D2. This transient voltage must be clamped at a voltage no **greater than 5V**. D3 and D4 act the same way when the transient is across the RX+/- differential pair. The total capacitance seen by each differential pair must not exceed 50pF (25pF single ended).

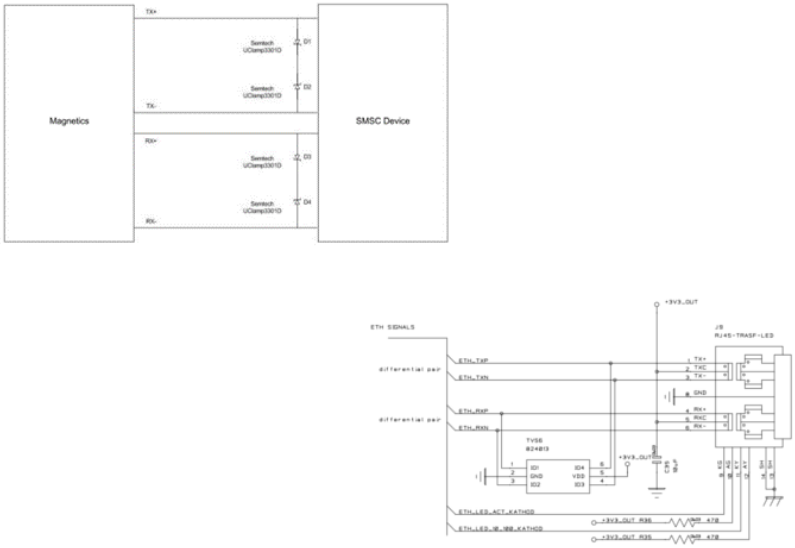


Figure 9

Recommended by ENGICAM:

Diode array TVS, 4 CH, ESD, 3.3V Wurth Elektronik 824013

Note: *for further details about PHY Protection reffer to file AN1718 of SMSC*

5.7 USB INTERFACE

5.7.1 HOW TO CONNECT THE USB OTG INTERFACE

The NXP ST USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. The figure shows how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. The following table lists all USB/OTG signal of mail connector.

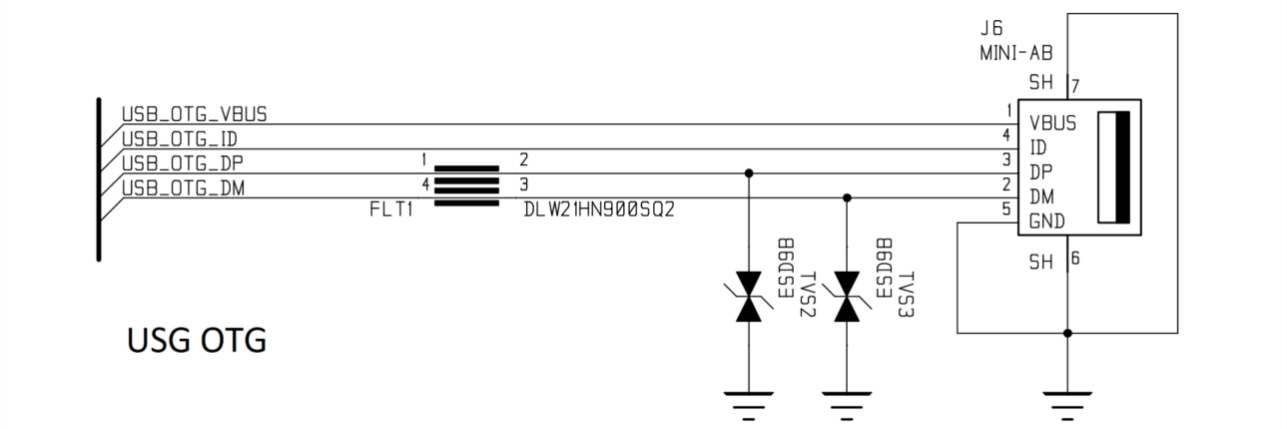


Figure 10

Number	Name	Primary Function Description	GPIO Capable	Voltage
195	USB_OTG_VBUS *	USB on the go interface	N	-
192	USB_OTG_DP	USB on the go interface	N	-
193	USB_OTG_DN	USB on the go interface	N	-
191	USB_OTG_ID	USB on the go interface	Y	-

Table 14

**** Note: The USB_OTG_VBUS is an INPUT power signal. It must be connected to 5V***

The following figures show two different ways to connect the USB OTG interface that may be used to work as either a host or a device.
Use of the USB OTG port as a Host with its own dedicated supply. The ID signal is forced to GND

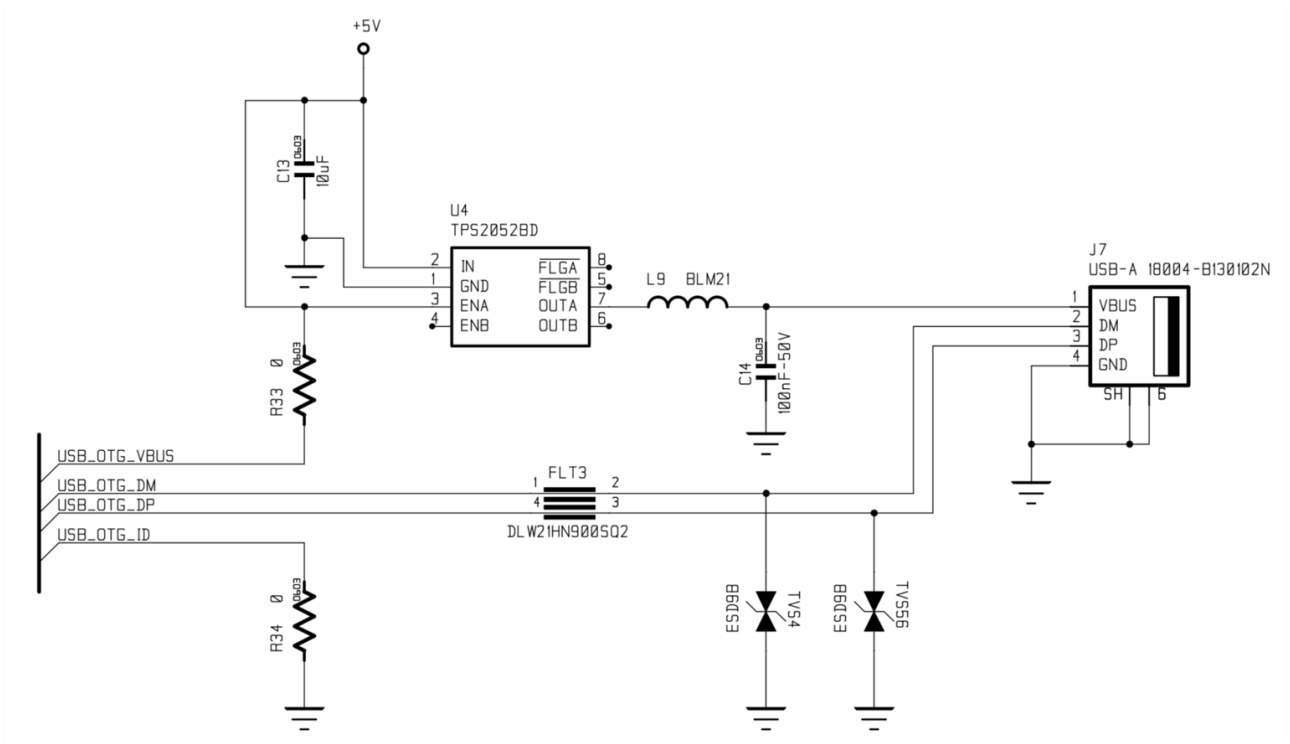


Figure 11

Use of the USB OTG port as Device.

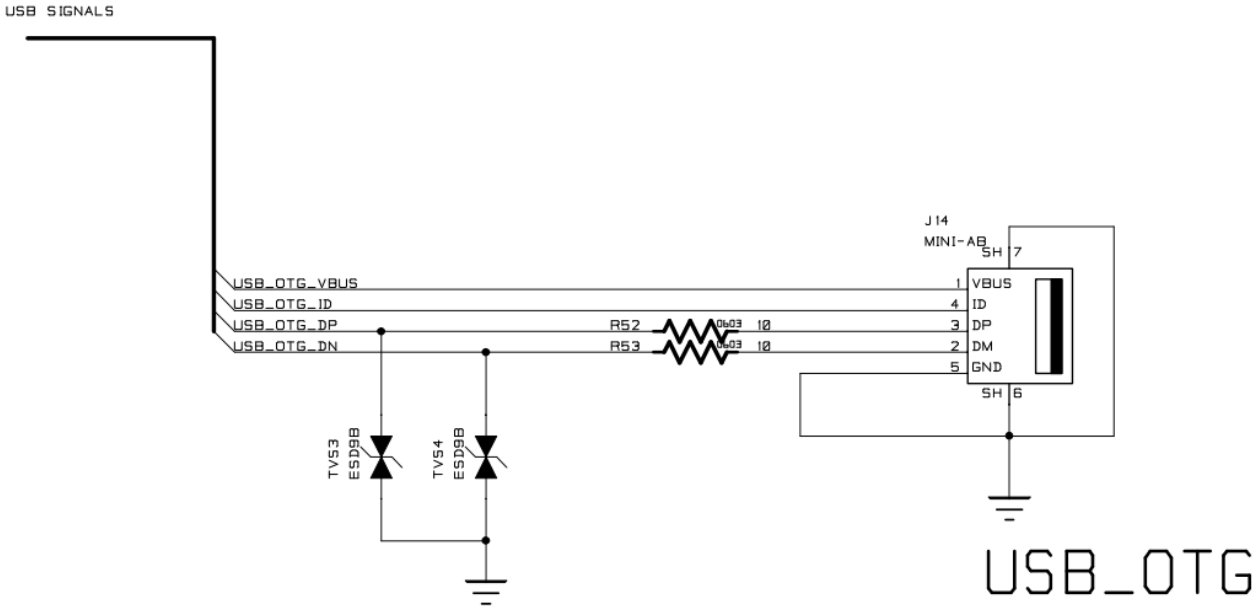


Figure 10

5.7.2 HOW TO CONNECT THE USB HOST INTERFACE

The module provides one port for USB host interface. The figure shows how to connect this port to the Module.

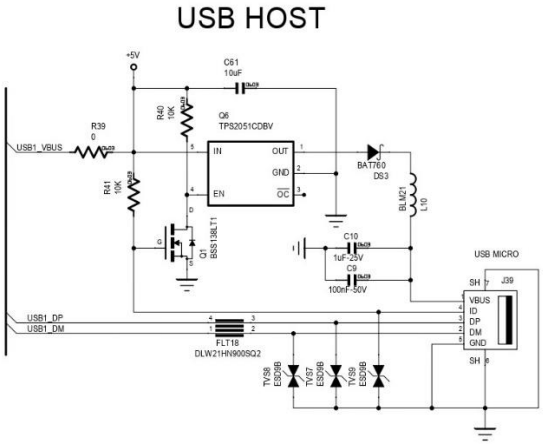


Figure 11

It's possible to multiply the USB ports available by equipping the carrier board with a USB HUB.

The Figure 12 shows how to connect USB Hub outputs to: USB power distribution switches (TPS 2052BD) and USB type A connector.

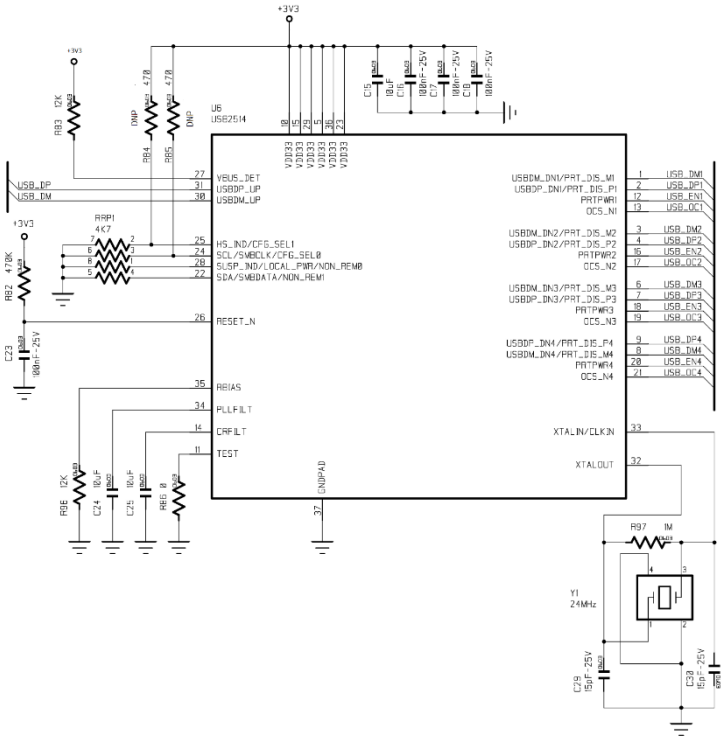


Figure 12

If only one port is needed it's possible to connect the USB_D (M/P) signals shown in the figure, directly to the module on pin 194-196 of the main connector.

Number	Name	Primary Function Description	GPIO Capable	Voltage
194	USB_H1_DP	USB HOST interface	N	-
196	USB_H1_DN	USB HOST interface	N	-

Table 15

**** Note: The USB_VBUS is an INPUT power signal. It must be connected to 5V***

5.8 HOW TO CONNECT THE SD CARD INTERFACE

The STM32MP1 provides the interface between the host system and MMC/SD/SDIO/CE-ATA cards, including cards with reduced size or mini cards. The module includes these features and the figure shows how the Micro SD Card connector is connected to ST Module in the evaluation board. The SD card signals of the module's main connector are listed in table below.

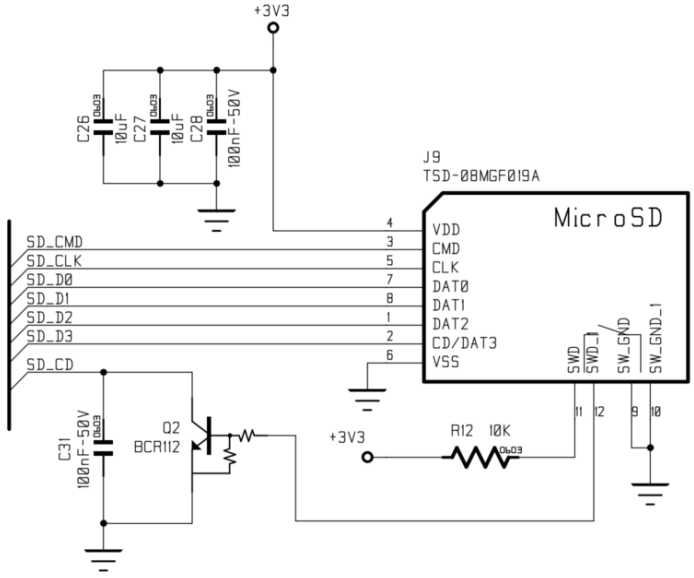


Figure 13

SDIO1 Interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
183	SDIO_A_nCD	SD CD Signal	Y	+3,3V
184	SD_WP (GPIO1_IO01)	SD WP Signal	Y	+3,3V
188	SDIO_A_DATA0	SD DAT 0 signal	Y	+3,3V
187	SDIO_A_DATA1	SD DAT 1 signal	Y	+3,3V
185	SDIO_A_DATA2	SD DAT 2 signal	Y	+3,3V
186	SDIO_A_DATA3	SD DAT 3 signal	Y	+3,3V
189	SDIO_A_CLK	SD CLK signal	Y	+3,3V
190	SDIO_A_CMD	SD CMD signal	Y	+3,3V

Table 16

SDIO2 Interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
37	SD2_nCD# (PI0)	SD 2 CD Signal	Y	+3,3V
35	SD2_WP (PH5)	SD 2 WP Signal	Y	+3,3V
166	SD0_B_DATA3	SD 2 DAT 3 signal	Y	+3,3V
167	SD0_B_CMD	SD 2 CMD signal	Y	+3,3V
168	SD0_B_DATA0	SD 2 DAT 0 signal	Y	+3,3V
169	SD0_B_CLK	SD 2 CLK signal	Y	+3,3V
170	SD0_B_DATA2	SD 2 DAT 2 signal	Y	+3,3V
171	SD0_B_DATA1	SD 2 DAT 1 signal	Y	+3,3V

Table 17

These pins are mapped on the same PADS, so the SDIO A and B are CANNOT be used simultaneously

5.9 HOW TO CONNECT AN LCD DISPLAY

The GEA STM32MP1 module offers LCD signals for 24 bit display. The pin names indicate the color mapping: for example LCD_B0 is relative to Blue LSB and B7 to Blue MSB.

Number	Name	Primary Function Description	GPIO Capable		Voltage
82	LCD _B0	LCD interface	Y		+3,3V
84	LCD _B1	LCD interface	Y		+3,3V
159	LCD _B2	LCD interface	Y		+3,3V
158	LCD _B3	LCD interface	Y		+3,3V
157	LCD _B4	LCD interface	Y		+3,3V
155	LCD _B5	LCD interface	Y		+3,3V
154	LCD _B6	LCD interface	Y		+3,3V
153	LCD _B7	LCD interface	Y		+3,3V
86	LCD _G0	LCD interface	Y		+3,3V
88	LCD _G1	LCD interface	Y		+3,3V
152	LCD _G2	LCD interface	Y		+3,3V
151	LCD _G3	LCD interface	Y		+3,3V
150	LCD _G4	LCD interface	Y		+3,3V
149	LCD _G5	LCD interface	Y		+3,3V
148	LCD _G6	LCD interface	Y		+3,3V
147	LCD _G7	LCD interface	Y		+3,3V
90	LCD_R0	LCD interface	Y		+3,3V
92	LCD_R1	LCD interface	Y		+3,3V
146	LCD _R2	LCD interface	Y		+3,3V
145	LCD _R3	LCD interface	Y		+3,3V
144	LCD _R4	LCD interface	Y		+3,3V
143	LCD_R5	LCD interface	Y		+3,3V
142	LCD_R6	LCD interface	Y		+3,3V
141	LCD_R7	LCD interface	Y		+3,3V
160	LCD _VSYNC	LCD interface	Y		+3,3V
161	LCD _HSYNC	LCD interface	Y		+3,3V
125	LCD _CLK	LCD interface	Y		+3,3V
162	LCD_DRDY	LCD interface	Y		+3,3V

Table 18

5.10 BOOT MODE PIN

Boot mode pin determines how the module boot. The following table listed the possible options of the boot mode:

BOOT_MODE	Action
0	Boot from memory devices
1	Boot from Serial[1)]

Table 19

[1)] The boot from Serial is usually used for the boot loader deploy, for further information referring to the CPU RM.

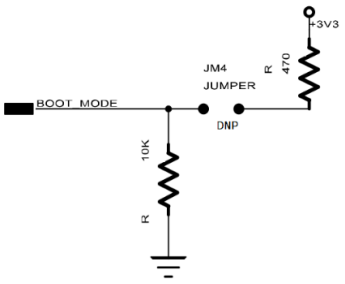


Figure 14

The table below lists the boot mode Pin numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
181	BOOT_MODE	Boot from Serial or Memory device	N	-

Table 20

Following image shows the set-up configurations for bootstrap from eMMC and from SD card.

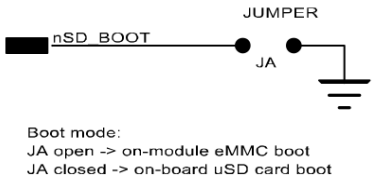


Figure 15

The signal used to configure the boot is implemented on pin 80. In the standard condition the signal is setting to boot from eMMC (jumper left open), closing the jumper the module start from SD card.
Following you can see the signals logical level to implement a custom starting sequence. The first sequence is already implemented in the module.

BOOT FROM Module's Memory Devices	
Signal on pin	LOGIC LEVEL
80	1

Table 21

The choice of boot from SD means short-cutting the jumper, you can have the same effect by pulling down directly the signal on pin 80.

BOOT FROM SD1	
Signal	LOGIC LEVEL
80	0

Table 22

Note: for using of any customized boot options refer to the NXP reference manual of STM32MP135

5.11 HOW TO CONNECT THE AUDIO INTERFACE

GEA STMP1 is equipped with a SAI (Synchronous Audio Interface) that can be connected with a standard audio codec device.
The figure below shows connection with a Low Power Stereo Codec using the module signals interface

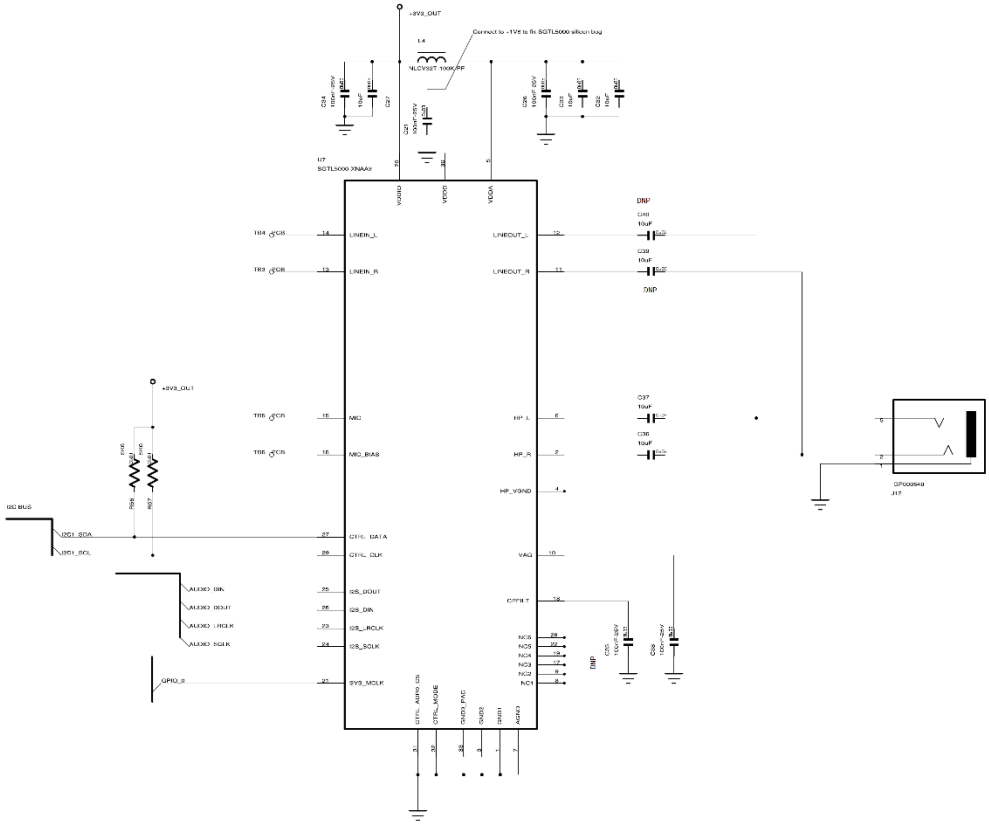


Figure 16

The following table lists the I2S BUS pins numbering

Number	Name	Primary Function Description	GPIO Capable	Voltage
114	SAI1_SDB	I2S Data In	Y	+3,3V
122	SAI1_SDA	I2S_Data OUT	Y	+3,3V
124	SAI1_SCKA	I2S_SCLK	Y	+3,3V
115	SAI1_FSA	I2S_LRCLK	Y	+3,3V

Table 23

WARNING!
To implement the SGTL5000 on the carrier board, remember to connect the VDD, pin 30 of the SGTL5000 device, to +1V8 to fix a silicon bug (for further detail refer to SGTL5000 data sheet)

5.12 HOW TO CONNECT THE RESET PIN

The nRESET signal has input/output functionality and shall be driven in open-drain mode. *The signal has an internal 100K pull-up; the maximum recommended capacitive load is about* ***100pF****.*

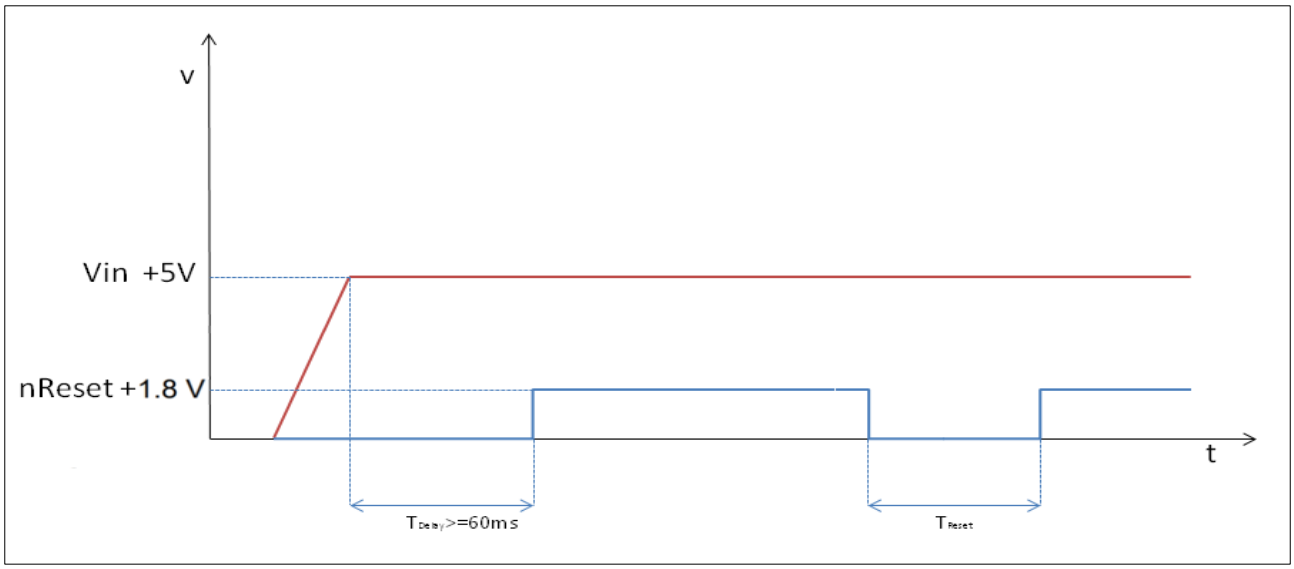


Figure 17

TDelay: driven low by SOM during the POR state
TReset: driven low by user to force POR CPU pin

5.12.1 INPUT MODE USAGE

The nRESET signal can be used to reset the module by driving it with an open-drain or with a simple button. If there are no special requirements, the module is fully auto-sufficient in terms of reset sequence, so its nRESET signal can be left floating. No Pull-up resistor is required on the carrier board; if a different pull-up resistor value (from the 100K on board of the module) is necessary, an additional pull-up on the carrier can be placed.

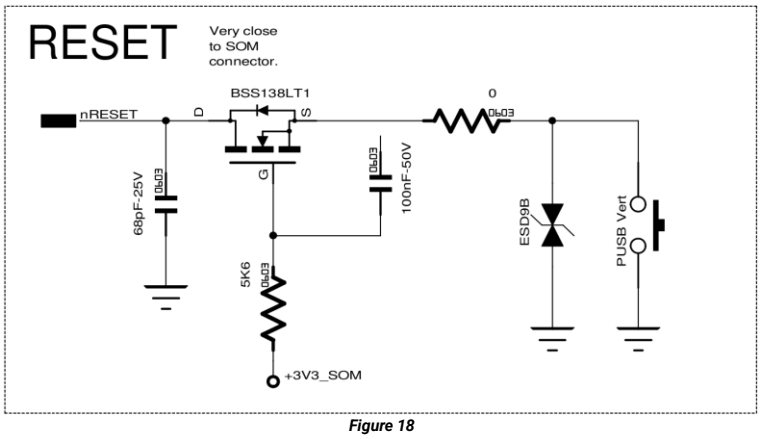


Figure 18

CHAPTER 6

PERIPHERAL MULTIPLEXING

This Chapter gives the alternative peripheral information

Section includes：

- **SPI**
- **I2S**
- **PWM**
- **I2C**
- **UART**
- **CAN**

6.1 PERIPHERAL MULTIPLEXING DESCRIPTION

In the following we describe opportunity to use alternative interfaces using the properties of multiplexing pin.
Refer to the NXP's reference manual and documentation for further details.

6.1.1 SPI & IIS CONFIGURATION

Using pin multiplexing 's features we may have the following SPI and IIS connections. The tables below show the output signals on the Connector's module.

SPI1 signals interfaces +3,3V

Pin number	Pin Name on MP135	Signal reference	Voltage reference
28 / 65	PA3 / PC0	MOSI	+3,3V
29 / 34	PA6 / PC3	MISO	+3,3V
30 / 34 / 184	PB1 / PC3 / PA7	SCK	+3,3V
27 / 122	PF12 / PA5	NSS	+3,3V

Table 24

SPI2 signals interfaces +3,3V

Pin number	Pin Name on MP135	Signal reference	Voltage reference
63 / 153	PH10 / PA8	MOSI	+3,3V
73 / 120	PB5 / PG1	MISO	+3,3V
72	PB10	SCK	+3,3V
68 / 148	PB13 / PH11	NSS	+3,3V

Table 25

SPI3 signals interfaces +3,3V

Pin number	Pin Name on MP135	Signal reference	Voltage reference
88 / 166-186	PF1 / PC11	MOSI	+3,3V
92 / 105 / 168-188	PG7 / PD4 / PC8	MISO	+3,3V
152 / 170-185	PH13 / PC10	SCK	+3,3V
151 / 167-190	PF3 / PD2	NSS	+3,3V

Table 26

SPI4 signals interfaces +3,3V

Pin number	Pin Name on MP135	Signal reference	Voltage reference
14 / 23	PE11 / PD1	MOSI	+3,3V
84 / 151	PE13 / PF3	MISO	+3,3V
132 / 162	PE12 / PH9	SCK	+3,3V
72 / 159	PB10 / PD10	NSS	+3,3V

Table 27

SPI5 signals interfaces +3,3V

Pin number	Pin Name on MP135	Signal reference	Voltage reference
33 / 108	PH3 / PH12	MOSI	+3,3V
147 / 153	PE4 / PA8	MISO	+3,3V
36 / 114	PH7 / PG10	SCK	+3,3V
8 / 148	PF10 / PH11	NSS	+3,3V

Table 28

The following tables show the pin configurations for IIS Bus on module's connector.

IIS2 bus interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
26 / 114	PG10 / PA0	I2S_DIN	+3,3V
27 / 116 / 122	PF12 / PD6 / PA5	I2S_DOUT	+3,3V
65 / 108 / 124	PC0 / PH12 / PA4	I2S_SCLK	+3,3V
14 / 115 / 147	PE11 / PF11 / PE4	I2S_LRCLK	+3,3V
32 / 34 / 119	PD13 / PC3 / PD0	I2S_MCLK	+3,3V

Table 29

IIS2 bus interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
121 / 169-189	PG3 / PC12	I2S_DIN	+3,3V
148 / 184	PH11 / PA7	I2S_DOUT	+3,3V
29	PA6	I2S_SCLK	+3,3V
66 / 120	PB0 / PG1	I2S_LRCLK	+3,3V
153	PA8	I2S_MCLK	+3,3V

Table 30

6.1.2 ALTERNATIVE PWM PINS TABLE

Following, a few possible alternate PWM pins. For further details please consult the ST RM

Pin number	Pin Name on MP135	Signal reference	Voltage reference
113 / 161	PF9 / PE9	TIM1_CH1	+3,3V
14 / 142	PE11 / PA9	TIM1_CH2	+3,3V
25 / 84 / 191	PA1 / PE13 / PA10	TIM1_CH3	+3,3V
162	PH9	TIM1_CH4	+3,3V
26 / 90 / 122	PA0 / PA15 / PA5	TIM2_CH1	+3,3V
25	PA1	TIM2_CH2	+3,3V
72	PB10	TIM2_CH3	+3,3V
28	PA3	TIM2_CH4	+3,3V
29	PA6	TIM3_CH1	+3,3V
73 / 184	PB5 / PA7	TIM3_CH2	+3,3V
68 / 168-188	PB0 / PC8	TIM3_CH3	+3,3V
30 / 171-187	PB1 / PC9	TIM3_CH4	+3,3V
154	PB6	TIM4_CH1	+3,3V
9 / 32	PB7 / PD13	TIM4_CH2	+3,3V
10 / 144	PB8 / PD14	TIM4_CH3	+3,3V
109	PD15	TIM4_CH4	+3,3V

Table 31

6.1.3 IIC CONFIGURATION

IIC1 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
10 / 170-185	PB8 / PC10	SCL	+3,3V
6 / 166-186	PE8 / PC11	SDA	+3,3V

Table 32

IIC2 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
111 / 158	PD7 / PF2	SCL	+3,3V
88 / 110 / 121	PF1 / PG9 / PG3	SDA	+3,3V

Table 33

IIC3 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
10 / 33 / 108	PB8 / PH3 / PH12	SCL	+3,3V
36 / 111 / 144 / 146 / 157	PH7 / PD7 / PD14 / PH8 / PH14	SDA	+3,3V

Table 34

IIC4 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
68 / 106 / 148	PB13 / PE15 / PH11	SCL	+3,3V
9 / 153	PB7 / PA8	SDA	+3,3V

Table 35

IIC5 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
23 / 152	PD1/ PH13	SCL	+3,3V
24 / 84 / 151	PH6 / PE13 / PF3	SDA	+3,3V

Table 36

6.1.4 ALTERNATIVE UART PINS TABLES

The following tables show an alternative UART configuration

UART1 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
65 / 142 / 154	PC0 / PA9 / PB6	UART1_TXD	+3,3V
32 / 66 / 144	PD13 / PB0 / PD14	UART1_RXD	+3,3V

Table 37

UART2 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
15 / 108 / 115 / 117	PF13 / PH12 / PF11/ PD8	UART2_TXD	+3,3V
28 / 109 / 146	PA3 / PD15 / PH8	UART2_RXD	+3,3V
14 / 106	PE11 / PE15	UART2_CTS	+3,3V
25 / 105	PA1 / PD4	UART2_RTS	+3,3V

Table 38

UART3 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
72 / 117 / 170-185	PB10 / PD8 / PC10	UART3_TXD	+3,3V
160 / 167-190	PG4 / PD2	UART3_RXD	+3,3V
63 / 141 / 168-188	PH10 / PD11 / PC8	UART3_CTS	+3,3V
171-187	PC9	UART3_RTS	+3,3V

Table 39

UART4 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
11 / 23 / 27 / 116 / 142 / 152	PA13 / PD1 / PF12 / PD6 / PA9 /PH13	UART4_TXD	+3,3V
10 / 12 / 30 / 90 / 117 / 157	PB8 / PE5 / PB1 / PA15 / PD8 / PH14	UART4_RXD	+3,3V
66	PB0	UART4_CTS	+3,3V
13 / 29 / 90	PE6 / PA6 / PA15	UART4_RTS	+3,3V

Table 40

UART5 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
26 / 68 / 145	PA0 / PB13 / PE7	UART5_TXD	+3,3V
15 / 73 / 166-186	PF13 / PB5 / PC11	UART5_RXD	+3,3V
171-187	PC9	UART5_CTS	+3,3V
168-188	PC8	UART5_RTS	+3,3V

Table 41

UART7 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
6 / 82 / 169-189	PE8 / PH2 / PC12	UART7_TXD	+3,3V
118 / 141	PE10 / PD11	UART7_RXD	+3,3V
92 / 113	PG7 / PF9	UART7_CTS	+3,3V
145 / 147	PB12 / PE4	UART7_RTS	+3,3V

Table 42

UART8 interfaces

Pin number	Pin Name on MP135	Signal reference	Voltage reference
112	PE1	UART8_TXD	+3,3V
113 / 155	PF9 / PE0	UART8_RXD	+3,3V

Pin number	Pin Name on MP135	Signal reference	Voltage reference
114 / 144	PG10 / PD14	UART8_CTS	+3,3V
132	PE12	UART8_RTS	+3,3V

Table 43

6.1.5 ALTERNATIVES CAN BUS INTERFACES

CAN 1 BUS Interface

Pin number	Pin Name on MP135	Signal reference	Voltage reference
114 / 118 / 171-187	PG10 / PE10 / PC9	CAN1_TX	+3,3V
110 / 119	PG9 / PD0	CAN1_RX	+3,3V

Table 44

CAN 2 BUS Interface

Pin number	Pin Name on MP135	Signal reference	Voltage reference
68 / 120 / 149	PB13 / PG1 / PG0	CAN2_TX	+3,3V
73 / 121 / 155	PB5 / PG3 / PE0	CAN2_RX	+3,3V

Table 45

CHAPTER 7

7.1 CARRIER BOARD RECOMMENDED SPECIFICATIONS

Following are the specifications required for the carrier board to avoid problems in the assembly process. The module is interfaced with the carrier board through a SO-DIMM with 200 positions connector type TYCO ELECTRONICS code 1473005-1 or compatible.
For proper assembly it is strongly recommended to paying attention to:

7.1.1 PLANARITY IN FINISH PROCESS

Due to the technical and mechanical specifications of the connector we suggest the maximum planarity of the footprint on PCB, so we suggest a type of finish obtained by horizontal process (we suggest and use for our carrier boards a type Chemical Gold finish).

7.1.2 PLANARITY OF PCB

Also, the planarity of the entire Printed Circuit Board must be kept in check especially when the carrier board grows in size. In this case we suggest you contact the manufacturer of PCB to understand how improve the planarity of ended board and optimize the process maintaining the electrical characteristics unchanged.

Note: for further detail refer to your SO-DIMM connector's data-sheet.

7.1.3 POWER SUPPLY

It's strongly recommended that the power supply of the carrier board, which feeds the driver and control devices connected with the STM processor, begins to work after the initialization of the processor itself.

CHAPTER 8

8.1 PRODUCT COMPLIANCE

In order to respect own internal policy regarding the environmental regulations and safety laws, Engicam in this chapter confirms the compliant, when applicable, of its own products to the normative ROHS and REACH and to the recognized hazards.

No hazard to report!